40(1991)February, No.1, Tokyo, Jap

U.D.C.681.325-181.48:621.3.049.774

High-Performance Single-Chip Microcontroller H8/300 Series

Nobuo Shibasaki*
Kenichi Ishibashi*
Kiyoshi Ogita**

ABSTRACT: Although single-chip microcontrollers are used widely in many applications, increased functionality and higher performance are constantly being demanded. The H8/300 series was developed as a new generation of single-chip microcontrollers. It has several advantages including high-speed, software production progress, an easy-to-use ZTAT™ concept, and easy family expansions for ASICs. The H8/300 series can offer embedded microcontrollers for small and middle size equipment that offer low-cost and high performance. The H8/300 CPU operates at high speed because it prefetches instructions and accesses its on-chip ROM and RAM through a 16-bit bus. Minimum instruction execution time is 0.2 μs at 10 MHz operation. By combining the high-speed CPU and the substantial peripheral functions, basic microcontrollers such as the H8/330 and the H8/325 and application specific type microcontrollers such as the H8/310 and the H8/350 are now available .

INTRODUCTION

THE single chip microcontroller is used in various product fields such as consumer products, industry equipment, and OA (office automation) equipment. The remarkable progress of the microcontroller application system and the increase in various equipment functions necessitates a product evolution with a high performance CPU. In the small and middle size equipment field, cost and performance are very important. Moreover, there are two significant tendencies in this field: one is providing more user-friendly facilities such as improved field-programmability; the other is manufacturing application specific ICs (ASICs) adding to the standard ICs.

Hitachi has developed the H8/300 series, a new generation 8-bit single chip microcontroller, which responds to these new and various needs.

THE H8/300 SERIES DEVELOPMENT CONCEPT

High-Speed CPU Operation

For performance improvement in application instruments, a high speed CPU is indispensable. The H8/300 CPU performs high speed operation. Basic operations between register and register, for example 16-bit addition/subtraction, take only 0.2 μs (at 10-MHz operation).

General registers

8 bits	8 bits
R0H	R0L
R1H	R1L
R2H	R2L
R3H	R3L
R4H	R4L
R5H	R5L
R6H	R6L
R7H (SP)	R7L

Control registers

PC

CCR	I	U	H	U	N	Z	V	C

SP: Stack pointer
PC: Program counter
CCR: Condition code register

Fig. 1—Register Configuration of the H8/300 CPU. The H8/300 CPU has eight 16-bit registers, a program counter, and a condition code register.

ZTAT™ Concept

Hitachi's original ZTAT™ concept can considerably reduce the time required for developing microcontroller

*Semiconductor Design & Development Center, Hitachi, Ltd.
**Application Engineering Department, Hitachi Microcomputer System Ltd.
ZTAT™ (Zero Turn Around Time) is a trademark of Hitachi, Ltd.

application systems. In the H8/300 series, the ZTAT™ version (the one-time PROM version) and mask ROM version have been developed and offered simultaneously. The ZTAT™ can be used not only in the development stage but also in small quantity production of many kinds of applications in the production stage.

Easy Family Expansion for ASICs

Hitachi's H8/300 series uses the SBP (silicon back plane) bus as the standard internal bus, and standardizes the on-chip peripheral function modules logically, electrically, and physically. Therefore, ASICs can be easily developed by the combination of on-chip peripheral modules and CPUs.

H8/300 CPU ARCHITECTURE AND FEATURES

General Register Architecture

Fig. 1 shows the register configuration of the H8/300 CPU. All general registers can be used as both data registers and address registers. When used as address registers, the general registers are accessed as 16-bit registers (R0 to R7). When used as data registers, they can be used for either 8-bit or 16-bit data registers. The H8/300 CPU, which employs this type of register architecture enables flexible and easy programming, as well as higher programming productivity. This is due to less restrictions of the architecture on the assignment of variables to registers during programming.

Simple Instruction Set for High Speed Operation

The following are the H8/300 CPU instruction set. The H8/300 CPU supports 57 instructions which consist of:

3 data transfer instructions
14 arithmetic instructions
4 logic instructions
8 shift instructions
14 bit manipulation instructions
5 branch instructions
8 system control instructions
1 block transfer instruction

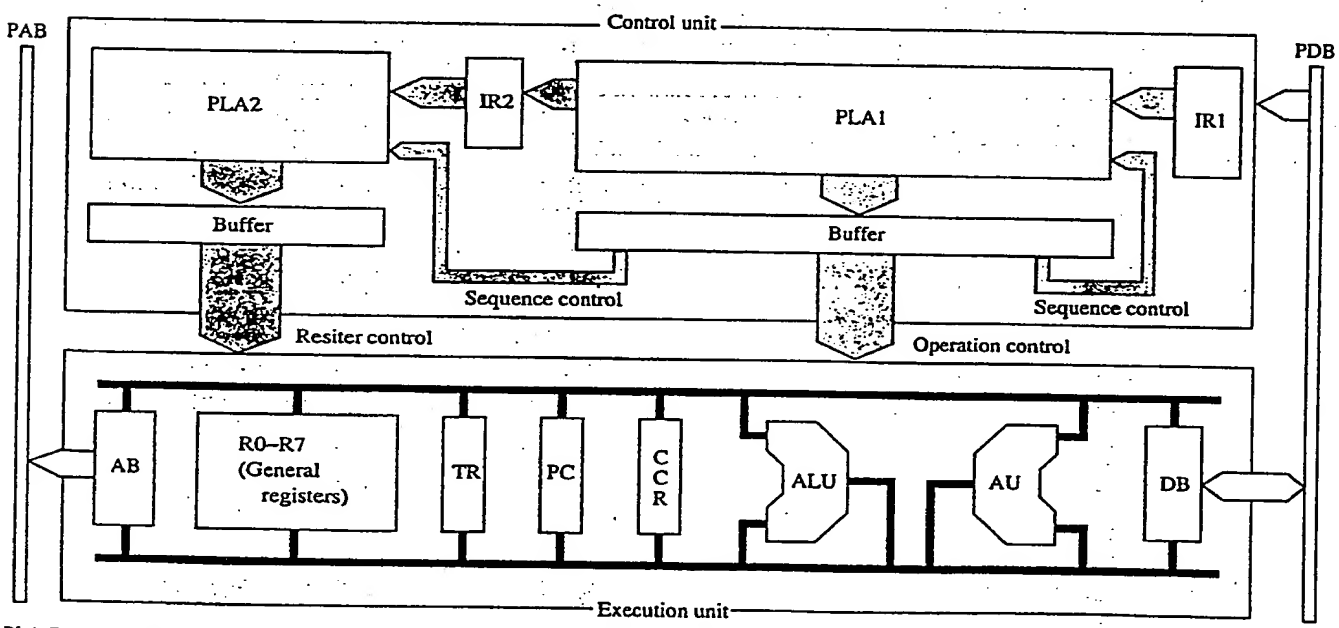
The H8/300 CPU operates them with high speed between registers. Memory can be accessed quickly by the data transfer instructions which can operate in many addressing modes. The outstanding instructions are as follows:

(1) Multiply and Divide Instructions

The H8/300 CPU supports multiply and divide instructions that are indispensable for control applications. 8-bit × 8-bit and 16-bit ÷ 8-bit operations are performed in high speed.

(2) Bit Manipulation Instructions

The H8/300 CPU has instructions which can set, clear, not, and test the bit data, and transfer and operate bit data between memory and carry bit of the CCR (Condition code



PLA:Programmable logic array
IR: Instruction register
AU:Arithmetic unit
ALU: Arithmetic and logic unit
TR: Temporary register
DB: Data buffer
AB: Address buffer
PDB: Internal data bus
PAB: Internal address bus

Fig. 2—Block Diagram of the H8/300 CPU.

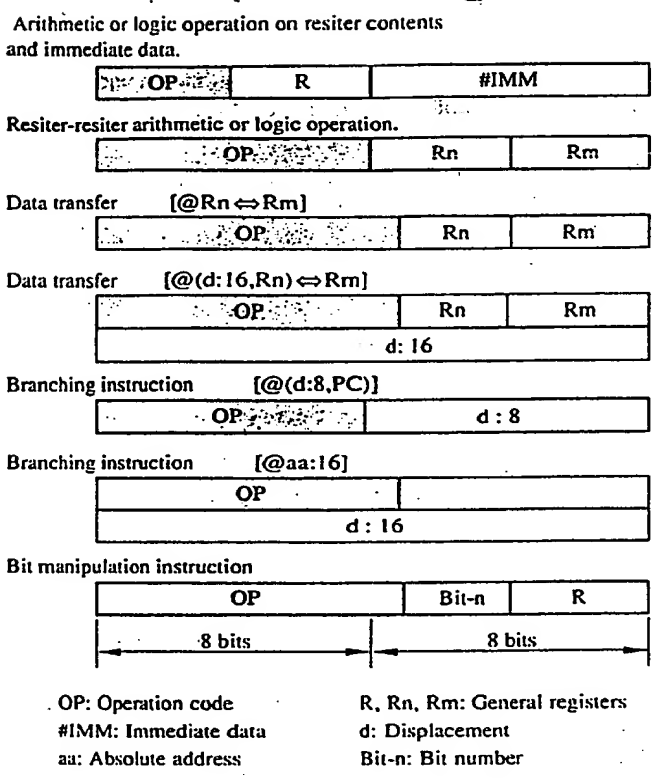


Fig. 3—The Instruction Format of the H8/300 CPU. The basic unit of instruction code is 2 bytes.

register). Bit operand is accessed by immediate data or register indirect. Consequently, these instructions enable complicated bit manipulation operations. As an example, on/off switching or software flag operation is easily achieved.

(3) Block Data Transfer Instruction

The block data transfer instruction performs the EEPROM write function for the H8/310, which has a large on-chip EEPROM (electrically erasable and programmable ROM). For others in the H8/300 series it is used as a block transfer instruction.

CPU Configuration

Fig. 2 shows the block diagram of the CPU. The control unit of the CPU is structured by PLA1 and PLA2. These PLAs decode the instructions and control the operation of the execution unit. The execution unit of the CPU is made up of registers and operation units.

(1) Internal Data Bus

The H8/300 CPU internal data bus (PDB) is 16 bits wide, and the interface between the CPU and the on-chip memory is operated in 16 bits. Therefore, the instruction is fetched at two bytes simultaneously, thus reducing the operation states of the two-byte instruction to one bus cycle.

(2) Instruction Format and Instruction Decoder

Fig. 3 shows the basic format of instructions. The basic unit of instruction code of the H8/300 CPU is 2 bytes, so the CPU does not need to determine whether the first address of instructions is an even or odd number. Also, the H8/300 CPU decodes 2 bytes simultaneously and can perform horizontal micro-instruction control at the PLAs. Consequently, the H8/300 CPU is compact and high speed.

(3) Pipeline Operation

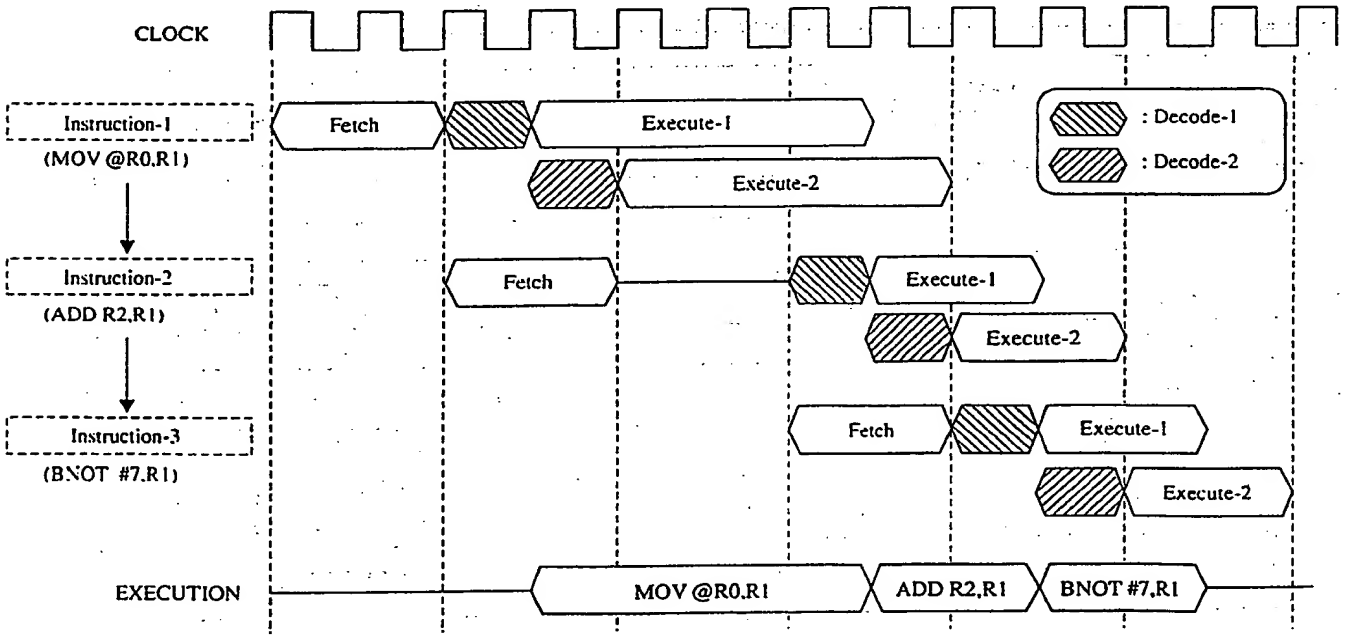


Fig. 4—The Operation Sequence of the H8/300 CPU. The H8/300 CPU uses a synchronous prefetch pipeline operation.

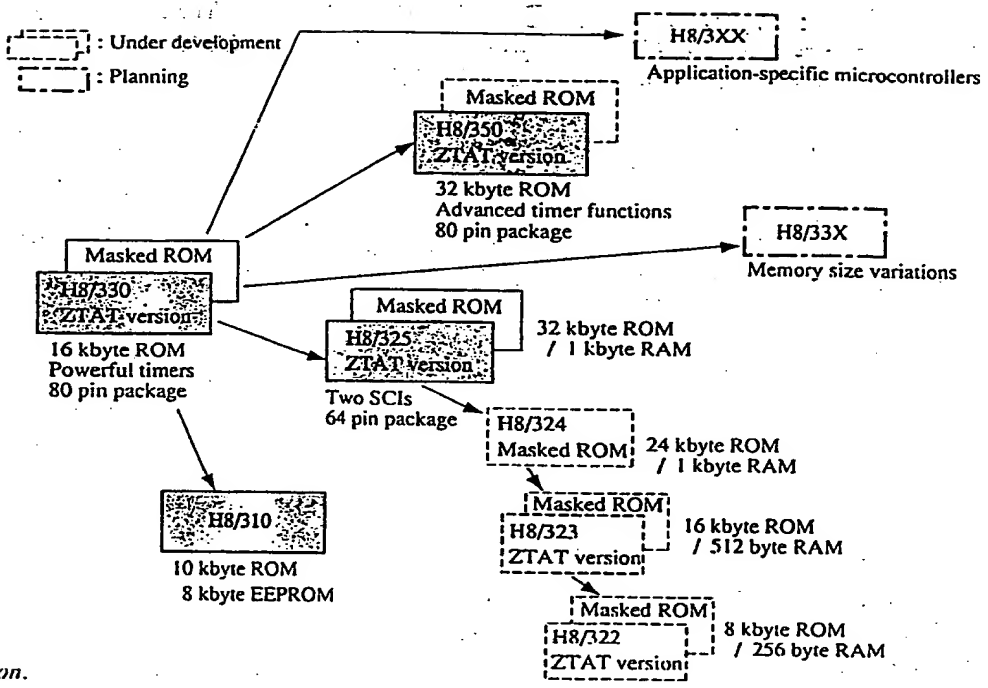


Fig. 5—The H8/300 Product Evolution.

Fig. 4 shows the operation sequence of the H8/300 CPU instruction. Instruction–2 is fetched immediately after the execution of instruction–1 has begun. At the end of the execution of instruction–1, instruction–2 is decoded and instruction–3 is fetched in parallel. The H8/300 CPU uses a synchronous prefetch pipeline operation. The decoding of the pipeline operations are functionally divided as two micro-instructions. Decode–1 and decod–2 are outputs of PLA1 and PLA2, respectively. PLA1 controls the operation and sequence (execution–1), and PLA2 controls the registers (execution-2). By repeating this operation, the instruction sequence is executed continuously.

As the result of (1), (2), and (3) the H8/300 CPU executes the operations between registers in one bus cycle and the data transfer between register and memory in two bus cycles.

TABLE 1. The Instruction Time of H8/300 CPU

The H8/300 CPU executes 43% of all the instructions at 0.2 μs at 10 MHz operation.

Operation *1)	8 bits	16 bits
Memory-register data transfer *2)	0.4 μs	0.4 μs
Register-register add/subtract	0.2 μs	0.2 μs
Register-register multiply/divide *3)	1.4 μs	—

*1) Single chip mode at 10 MHz

*2) RAM access in register-indirect addressing mode

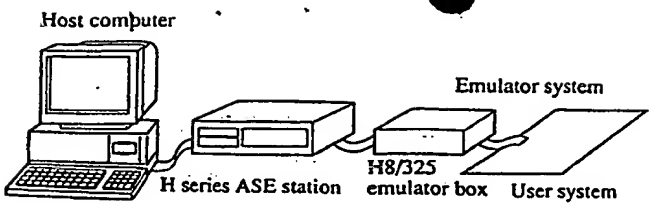
*3) 8 bits × 8 bits, 16 bits ÷ 8 bits

(4) High-Speed Branching Instructions

A branching instruction needs at least two bus cycles since the prefetch is invalid. Particularly, the relative branching instruction requires three bus cycles when the branching address is normally calculated after starting its instruction. Since the H8/300 CPU performs prefetching, necessary data for the branching is prepared just before the branching instruction, so the H8/300 CPU can calculate the branching address in the last state of the previous instruction. Arithmetic unit (AU) is used for branching address calculation which is independent from the arithmetic and logical unit (ALU). That is, in the last state of every instruction, AU calculates the branching address in parallel with the operation in the ALU, assuming that the next instruction is the branching instruction.

In addition to this, when executing the branch instruction the H8/300 CPU fetched the instruction from the branching address, regardless if the condition is met or not. The condition is determined during fetching, and if it coincides, instruction from the branching address is decoded and executed, and if the condition does not coincide, the instruction from the branching address is not executed and the previously fetched next instruction of branching instruction is executed.

The H8/300 CPU enables instructions which appear frequently to execute in one or two bus cycles. By shortening the execution states of many instructions, the number of micro-instructions are reduced, thus decreasing the scale of the control logic (mainly the PLA1).



Support software	Support hardware
•C compiler	•ASE station (one station serves entire H series)
•Assembler	•Emulator box
•Linkage editor	
•Librarian	
•Object converter (SYSROF to S type)	
• Simulator/debugger	

Fig. 6—H8/300 Series Support System.
The H8/300 series has an integrated environment for all stages of application system development, from program development through in-circuit debugging.

High-Speed Data Processing

As mentioned, the H8/300 CPU performs 16-bit access of on-chip memory and pipelining, along with a minimum instruction execution time of 0.2 µs* at 10-MHz operation. Table 1 shows an example of the H8/300 CPU instruction execution time. The H8/300 CPU executes 43% of all the instructions in 0.2 µs.

H8/300 SERIES PRODUCT EVOLUTION

Fig. 5 shows the H8/300 product evolution.

The H8/330 integrates 16k-byte ROM, 512-byte RAM, and powerful peripheral on-chip functions in an 80-/84-pin package. For peripheral functions, one channel of 16-bit free-running timer (4 input captures and 2 output compares), two channels of 8-bit timer (2 compares), and two channels of 8-bit PWM (pulse width modulation) timers are included. Using these timers, complicated input/output pulses can be enabled. Furthermore, the H8/330 has eight channels of 8-bit A/D converter, one channel of SCI (serial communication interface) which is programmable between synchronous or asynchronous mode, and 15-byte DPRAM (dual port RAM). Particularly, the DPRAM can transfer data at high speed to-from an external CPU with simple control signals. The H8/330 is used for applications which require high speed processing and sequence control such as automobiles, LBPs, and cameras. By using the H8/330 as a slave microcontroller, a multi-microcontroller system is easy to build.

The H8/325 series microcontroller is the basic model in the H8/300 series, and the package is an easy-to-mount 64-pin shrink DIP (dual inline package). The H8/325 series all have the same peripheral functions. Memory size differs among other products, however, (H8/322), so the user can select the mo... depending on their program size.

The H8/350 microcontroller is an 80-/84-pin ... with large on-chip memory and a powerful timer wi...

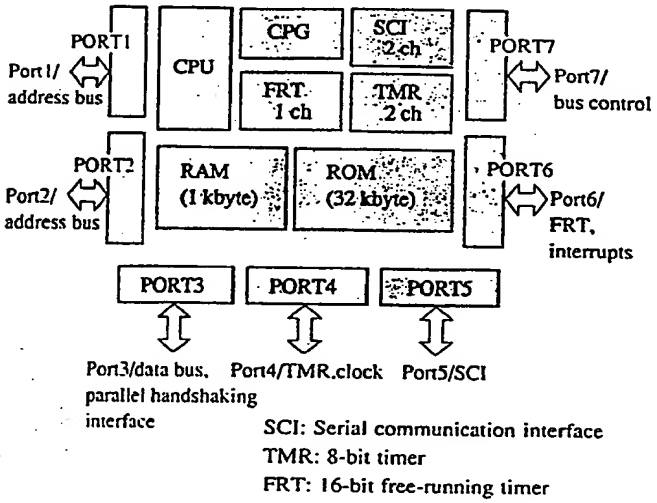
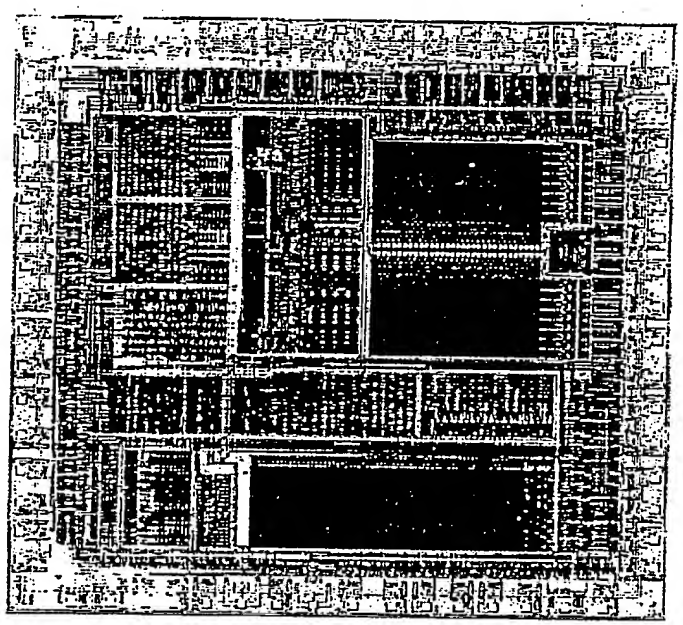


Fig. 7—Block Diagram of the H8/325.
The H8/325 has 32-kbyte ROM, 1-kbyte RAM, one 16-bit free-running timer and two 8-bit timers. Interrupts can be generated from 17 on-chip sources and four external interrupt lines.



H8/325 (Mask ROM)
HD6433258 (Die Size 6.95 × 7.03 mm)

Fig. 8—Photograph of the H8/325 (HD6433258) Chip. 400,000 transistors are integrated onto a 7.0 × 7.0 mm chip using the 1.0 µm CMOS process.

* The minimum instruction execution time of the H8/310 is 0.4 µs.

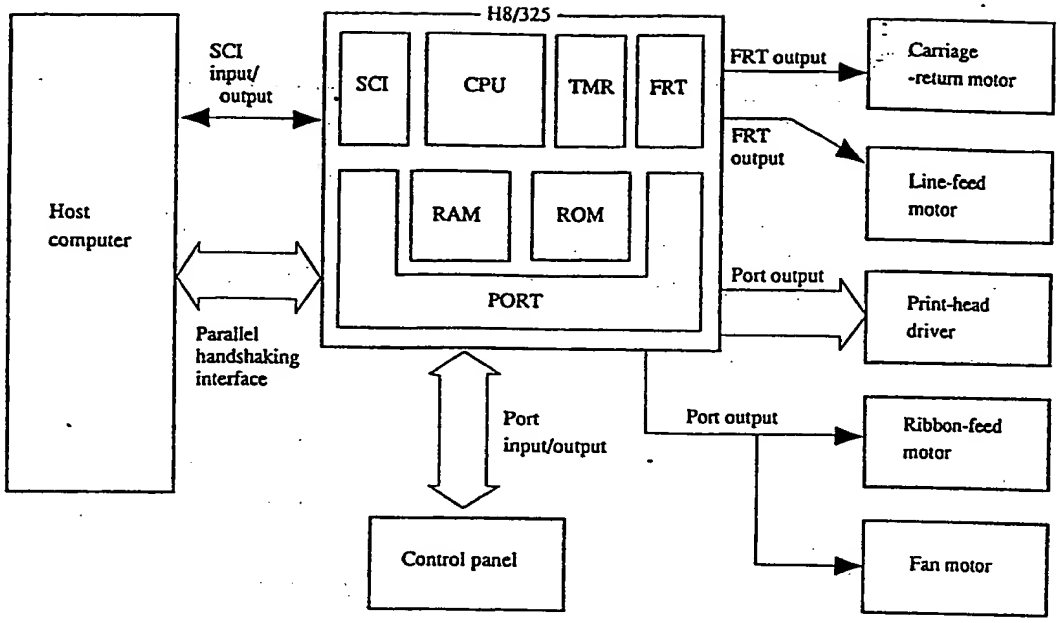


Fig. 9—Application Example of the H8/325: Printer. The H8/325 is a high-performance single chip microcomputer ideally suited for embedded control applications.

performs outstanding timing control. For timer function, there are six channels of 8-bit timer, one channel of 19-bit free-running timer, two channels of 16-bit timer, and two channels of 14-bit PWM timer. An internal timer network interconnects these timers. Therefore, many functions such as multi-wave outputs synchronized to the signal inputs are available. Furthermore, the H8/350 has one channel of 8-bit SCI, one channel of 16-bit clock synchronous mode SCI, and 16 channels of 8-bit A/D converter. By using these features, the H8/350 can be used for various control systems such as a sophisticated VCR (video cassette recorder) servo control system.

The H8/310 which is designed for use in IC cards has on-chip EEPROM. This single chip microcontroller has 8k-byte of EEPROM, 10k-byte ROM, and 256-byte RAM on a die size of 5 mm × 5 mm. The H8/310 has a high-level security system which protects the on-chip EEPROM and ROM from unauthorized access.

DEVELOMENT ENVIRONMENT

Fig. 6 shows a typical example of the development system configuration. A personal computer, workstation, or microcontroller can be connected and used as a host computer. To reduce the user's investment in development tools, the real time emulator is divided into a body common to all H8/300 series (ASE station) and an emulator box dedicated to one of H8/300 series LSIs. Therefore, when the user debugs another member of the H8/300 series, only the emulator box has to be replaced.

APPLICATION EXAMPLES

The application examples of the H8/325 are described below. Fig. 7 shows a block diagram and Fig. 8 shows a photograph of the H8/325. The H8/325 is used as an embedded microcontroller in various product fields such as OA equipment, consumer products, and industry equipment. Fig. 9 shows the application example in a printer.

CONCLUSIONS

The H8/300 series, a new generation high performance single chip microcontroller was developed and described, especially with regard to the unique features of its CPU architecture that achieves high speed operation and its powerful four new microcontrollers that improve the cost performance of application products. In the application fields of small and middle size equipment, more and more cost-performance and ease of use is required.

We plan to expand the H8/300 series products and respond to these needs continuously.

REFERENCES

(1) H8/330 Programming Manual, Hitachi, Ltd.(1989).
(2) H8/330 Hardware Manual, Hitachi, Ltd.(1989).
(3) S Baba et al., "High-Peformance Single-chip Microcontroller H8 Series," *Hitachi Review*, 38, 1(1989).